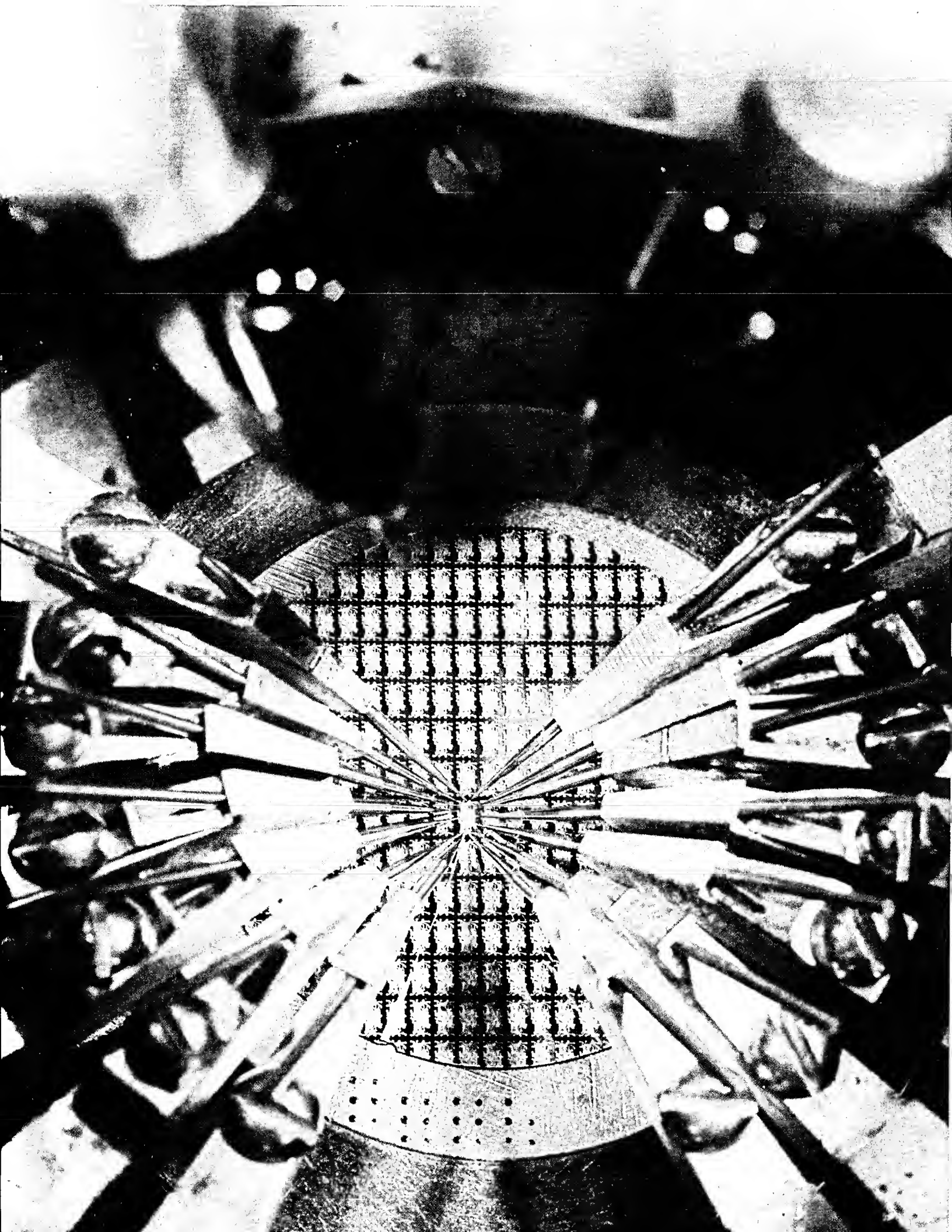
Sylvania universal high level logic integrated circuits

SYLVANIA



Sylvania Integrated Circuits

In the time that Sylvania's two lines of integrated circuits have been available, both SUHL* I and, SUHL* II have proven to be the highest quality saturated transistor-transistor logic available in the industry.

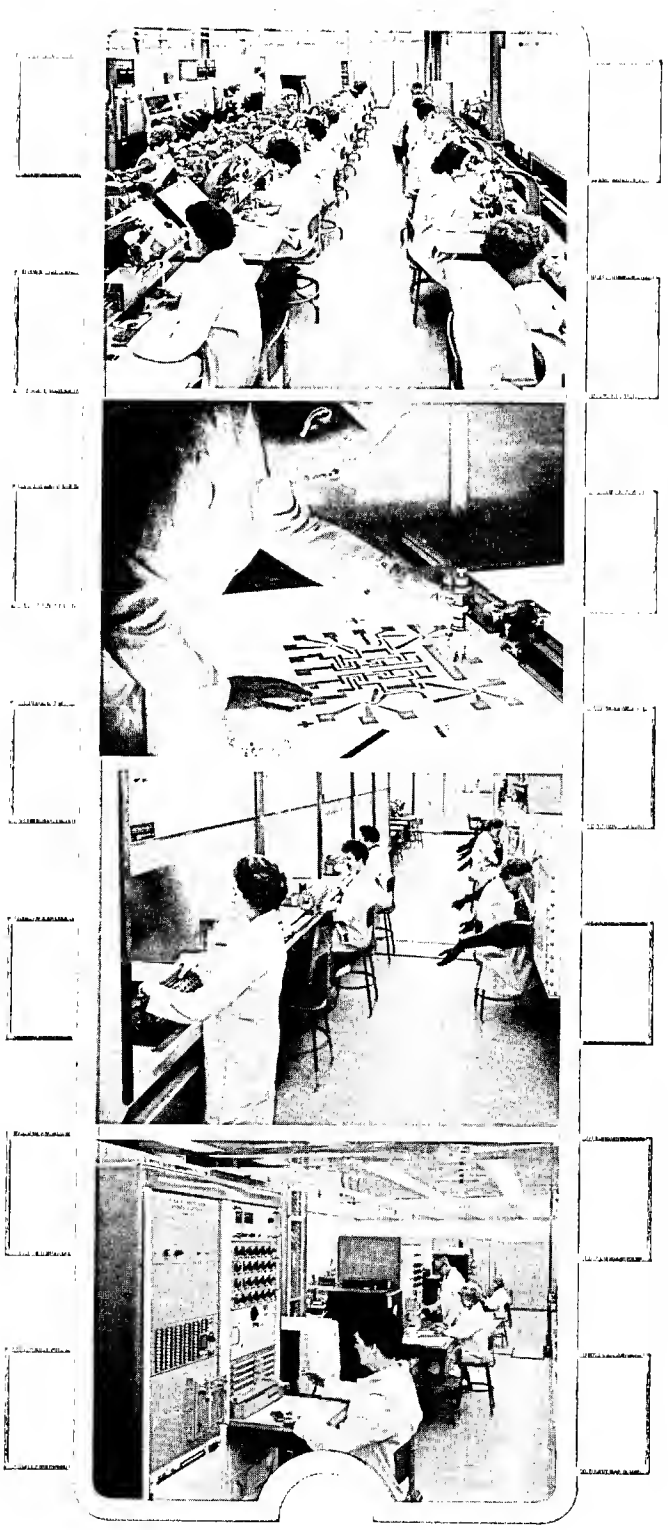
By early 1965, Sylvania had developed several series of circuits using the unusually efficient basic SUHL I circuit. The computer industry found that it was a low-cost, extremely reliable line that reduced can counts without compromising even the severest systems requirements. Today, SUHL I circuits are providing designers with the largest selection of compatible digital functions designed especially for tomorrow's computer systems.

Then in August, 1965, Sylvania announced SUHL II, the first integrated circuit line that satisfies extreme high-speed requirements while allowing all other vital characteristics to maintain their full levels of efficiency. Previously, several other manufacturers had reached comparable speeds, but only at the cost of tradeoffs in noise immunity, logic levels, power drain, temperature stability, fan-out vs. fan-in, or capacitance drive.

Both SUHL lines are characterized by high noise margin, fast speed, high logic swing, high fan-out, low power and capacitance drive capability. And both SUHL lines are interchangeable, pin-for-pin. SUHL is the fastest saturated logic family available today for applications down to 5 nanoseconds.

The diagrams and other information on the following pages provide important facts on all Sylvania SUHL circuits.

Sylvania Universal High level Logic



Automated 14-point probe test.

This is SUHL I ...Industry's Most Complete Line of TTL

The SUHL TTL integrated circuit line is designed to serve all logic requirements of typical computer systems.

All SUHL circuits are characterized into two temperature ranges: −55°C to +125°C for military applications and 0°C to +75°C for industrial and commercial use. Further, the designer has a choice of standard or prime fanout capability within each temperature range. All other electrical parameters and all pin connections are compatible, thereby allowing a single logic-system design to be applicable to either military or industrial markets. And, all SUHL I circuits are designed for applications up to and including 20 megacycles, with gate propagation delays in the range of 10 nanoseconds.

High Noise Immunity

Every circuit in the line contains an additional level-shifting transistor to permit positive or negative noise immunity of over 1 volt at 25°C and 500 mv at 125°C. Operating on a single power supply of +5.0 volts, the circuits provide a logic swing of greater than 3 volts.

High Fan-Out

As a direct result of Sylvania's buried-layer diffusion process, all SUHL integrated circuits have output transistors with very low Vce(SAT).This provides fan-out capability as high as 20, with various types ranging from 6 minimum to 16 minimum. The unique design of the line driver provides fanouts as high as 40 without sacrifice of speed or noise immunity. An active transistor pull-up network in the output of each circuit allows rapid charging of capacitance loads. The output is at very low impedance in either the ON or OFF state, which greatly minimizes the pick up of noise. Also, absolute short-circuit protection is built into every circuit as a result of a series resistor in the pull-up network.

Low Power Dissipation

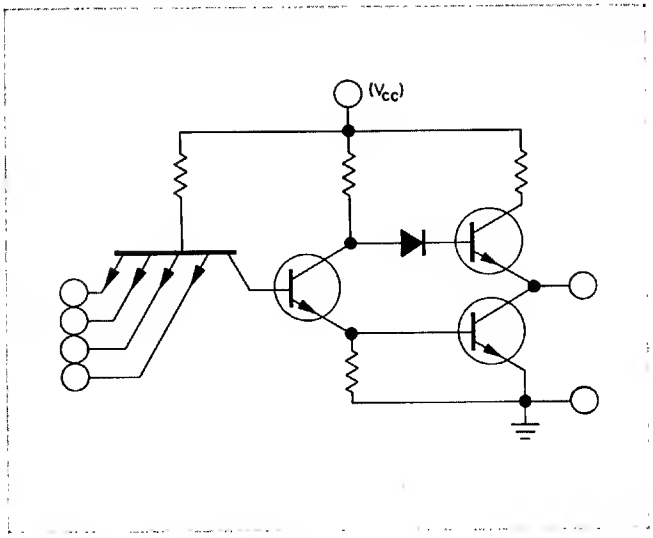
All SUHL circuits are designed with an extremely low speed-power product. With 20 megacycle switching speeds, the power dissipation per gate is only 15 milliwatts—a direct benet of Sylvania's ultra-fine masking technology. In addition, all circuits have transistor-transistor logic inputs which provide the logic capabilities and features of conventional diode-transistor logic, but offer considerably higher speed than DTL inputs.

High Fan-In

By utilizing low cost expanders, SUHL integrated circuits are able to provide fan-in capabilities as high as 18. Use of optimized TTL input geometries and special processes keep input leakage currents very low. These currents have a minimal effect on the logic "1" level of the driving gate due to the self compensating effect of the active pull-up network. Further, the level-shifting amplifier circuit between the input and output of the gate provides complete independence of fan-in from fan-out, eliminating the need for interaction rules.

Sylvania's optimum utilization of the combination of buried-layer diffusion and epitaxy results in very low Vce (SAT), low capacitance, high voltage breakdowns and very high frequency performance. Extremely small geometries and dimensional tolerances on the order of one-half micron (.00002"), make the parasitic capacitances so small they are less than equal to the stray capacitances of equivalent discrete component circuits.

SUHL I Basic Circuit

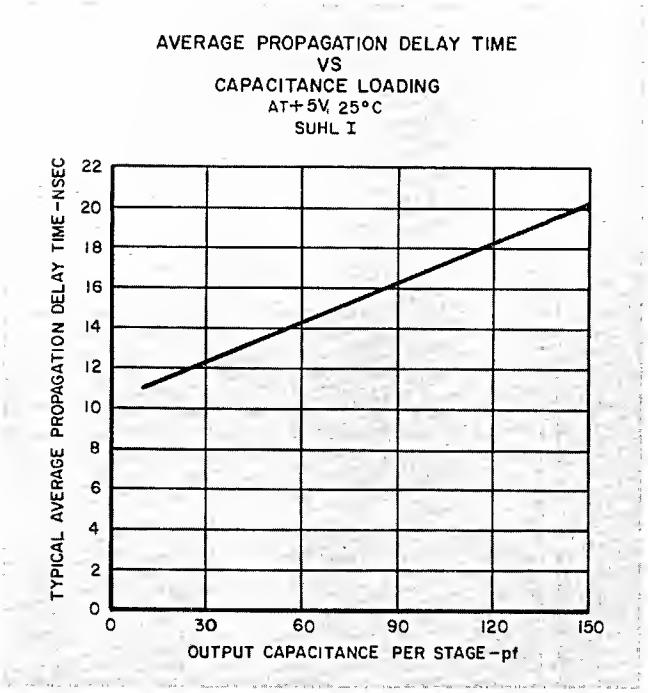


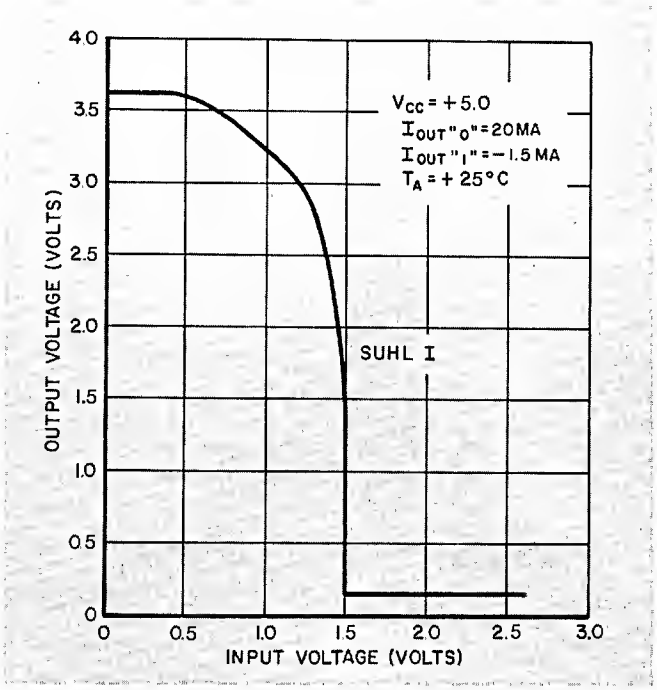
Typical Characteristics (+25°C, +5.0V)

SUHL I TYPICAL CHARACTERISTICS (+25°C, +5.0 volts)

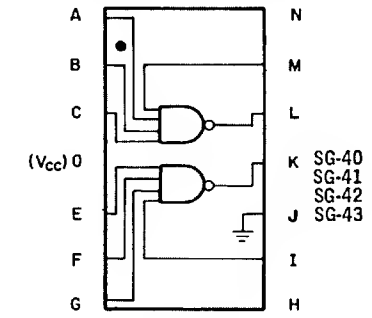
Function	Type Nos.	tpd (nsec)	Avg. Power (mw)	Noise Immunity +(volts)−		Military (−55° to +125°C) Prime FO	Military (−55° to +125°C) Std. FO	Industrial (0°C to +75°C) Prime FO	Industrial (0°C to +75°C) Std. FO
Dual 4-Input NAND/NOR GATE	SG-40, SG-41, SG-42, SG-43	10	15	1.1	1.5	15	7	12	6
Expandable Quad 2-Input OR Gate	SG-50, SG-51, SG-52, SG153	12	30	1.1	1.5	15	7	12	6
Single 8-Input NAND/NOR Gate	SG-60, SG-61, SG-62, SG-63	12	15	1.1	1.5	15	7	12	6
Exclusive-OR with Complement	SG-90, SG-91, SG-92, SG-93	11	35	1.1	1.5	15	7	12	6
Expandable Triple 3-Input OR Gate	SG-100, SG-101, SG-102, SG-103	12	25	1.1	1.5	15	7	12	6
Expandable Dual 4-Input OR Gate	SG-110, SG-111, SG-112, SG-113	12	20	1.1	1.5	15	7	12	6
Expandable Single 8-Input NAND/NOR Gate	SG-120, SG-121, SG-122, SG-123	18	15	1.1	1.5	15	7	12	6
Dual 4-Input Line Driver/ Lamp Driver	SG-130, SG-131, SG-132, SG-133	25	30	1.1	1.5	30	15	24	12
Quad 2-Input NAND/NOR Gate	SG-140, SG-141, SG-142, SG-143	10	15	1.1	1.5	15	7	12	6
Quad 2-Input OR Expander	SG-150, SG-151, SG-152, SG-153	4	20	1.1	1.5				
Triple 2-Input Bus Driver	SG-160, SG-161, SG-162, SG-163	15	15	1.1	1.5	15	7	12	6
Dual 4-Input OR Expander	SG-170, SG-171, SG-172, SG-173	3	5	1.1	1.5				
Dual 4-Input AND Expander	SG-180, SG-181, SG-182, SG-183			1.1	1.5				
Triple 3-Input NAND/NOR Gate	SG-190, SG-191, SG-192, SG-193	10	15	1.1	1.5	15	7	12	6
Set-Reset Flip-Flop	SF-10, SF-11, SF-12, SF-13	20mc	30	1.1	1.5	15	7	12	6
Two-Phase SR Clocked Flip-Flop	SF-20, SF-21, SF-22, SF-23	20mc	40	1.1	1.5	15	7	12	6
Single-Phase SRT Flip-Flop	SF-30, SF-31, SF-32, SF-33	12mc	30	1.1	1.5	15	7	12	6
J-K Flip-Flop (AND Inputs)	SF-50, SF51, SF-52, SF-53	20mc	40	1.1	1.5	15	7	12	6
J-K Flip-Flop (OR Inputs)	SF-60, SF-61, SF-62, SF-63	20mc	50	1.1	1.5	15	7	12	6

Typical curves

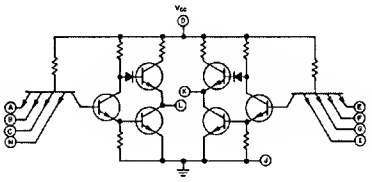




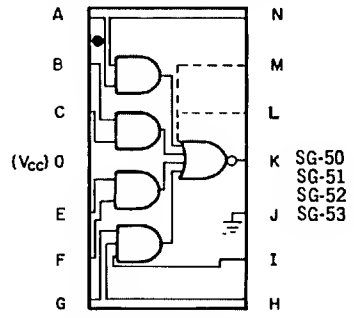
Dual 4-Input NAND/NOR Gate



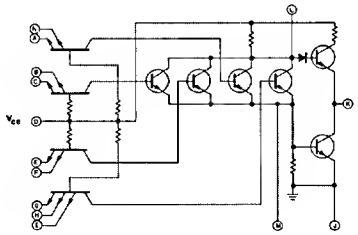
$L=\overline{(A\cdot B\cdot C\cdot M)}$
$K=\overline{(E\cdot F\cdot G\cdot I)}$



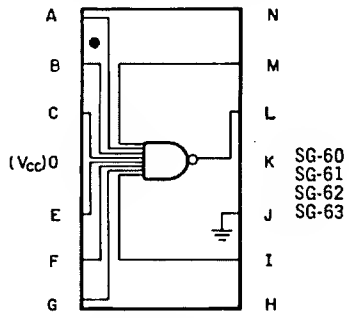
Expandable Quad 2-Input OR Gate



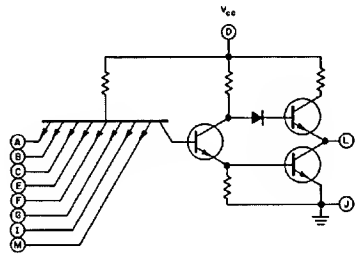
$K=\overline{(A\cdot N)+(C\cdot B)+(E\cdot F)+(G\cdot H\cdot I)}+--$



Single 8-Input NAND/NOR Gate



$L=\overline{(A\cdot B\cdot C\cdot E\cdot F\cdot G\cdot I\cdot M)}$

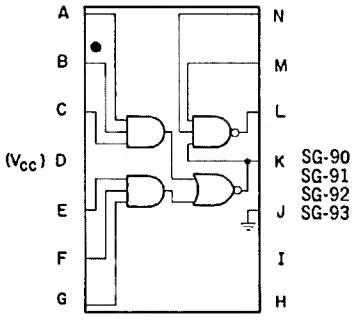


General Characteristics for all SUHL I Elements

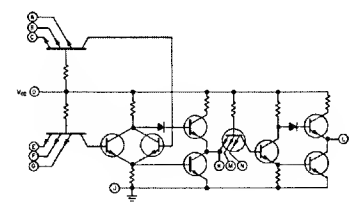
ABSOLUTE MAXIMUM RATINGS				
	Military	Industrial		Unit
Supply Voltage	8	7		Vdc.
Operating Temperature	−55° to +125°	0° to +75°		°C
Storage Temperature	−65° to +200°	−65° to +200°		°C
Electrical Characteristics at 25° C, Vcc = 5V				
INPUT CHARACTERISTICS	**Min.**	**Typ.**	**Max.**	**Unit**
Logic 1 Voltage	1.7		5.5	Volts
Logic 1 Current			100	μA
Logic 0 Voltage			1.2	Volts
Logic 0 Current		1.0		mA
Capacitance		2.0		pf
Positive Noise Immunity[1]	1.0			Volts
Negative Noise Immunity	1.0			Volts
Frequency		20		mcs
OUTPUT CHARACTERISTICS	**Min.**	**Typ.**	**Max.**	**Unit**
Logic 1 Voltage[2]	3.0	3.5	3.8	Volts
Logic 0 Voltage		0.26	0.45	Volts
Short Circuit Output Current	10		45.0	mA
Propagation Delay Time/Gate (varies with element designed to be used up to 20 mc)		10	20	ns
Fan-Out	*varies with elements designed for fan-outs of 6 to 30*			

1. Noise immunity is that voltage superimposed on the input which will not propegate beyond the following stage. ■ 2. With max Logic 0 on input.

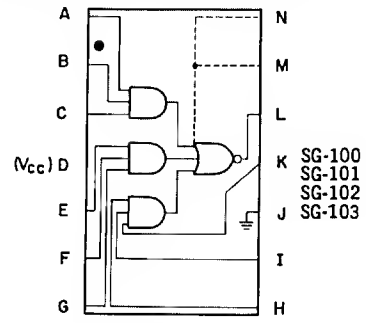
Exclusive-OR with Complement



$K=\overline{(A\cdot B\cdot C)+(E\cdot F\cdot G)}$
$L=\overline{(K\cdot M\cdot N)}$

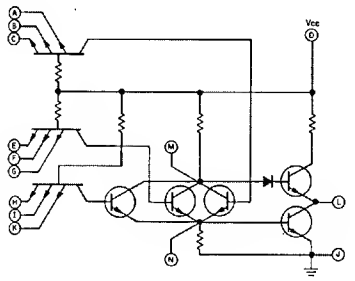


Expandable Triple 3-Input OR Gate

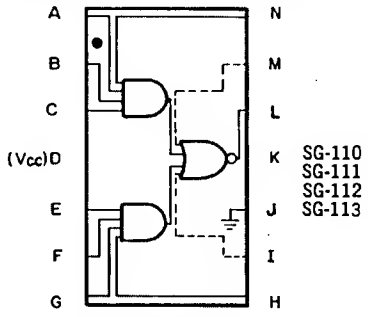


SG-100
SG-101
SG-102
SG-103

$L = \overline{(A \cdot B \cdot C) + (E \cdot F \cdot G) + (H \cdot J \cdot K) + \cdots}$

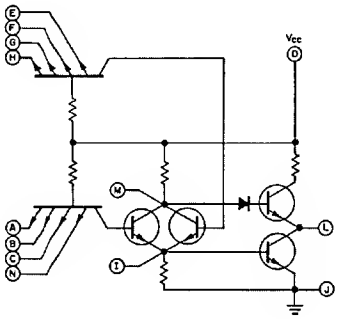


Expandable Dual 4-Input OR Gate

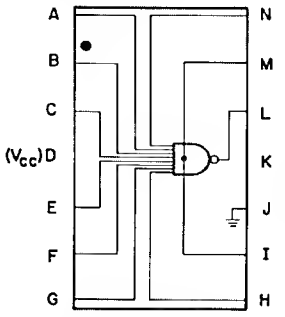


SG-110
SG-111
SG-112
SG-113

$L = \overline{(A \cdot B \cdot C \cdot N) + (E \cdot F \cdot G \cdot H) + \cdots}$

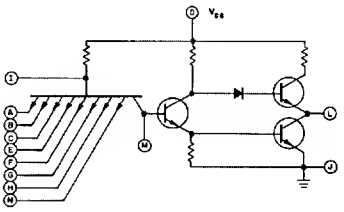


Expandable Single 8-Input NAND/NOR Gate

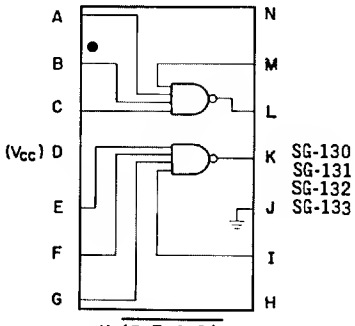


SG-120
SG-121
SG-122
SG-123

$L = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \; N \cdot \cdots}$



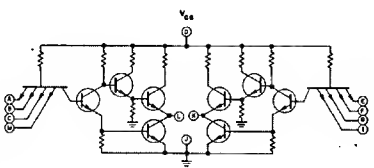
Dual 4-Input Line Driver/Lamp Driver



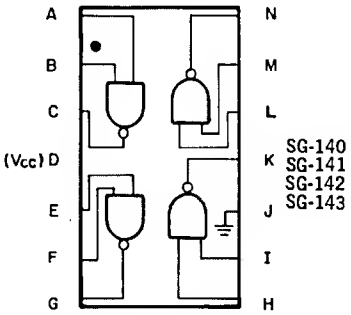
SG-130
SG-131
SG-132
SG-133

$K = \overline{(E \cdot F \cdot G \cdot I)}$

$L = \overline{(A \cdot B \cdot C \cdot M)}$



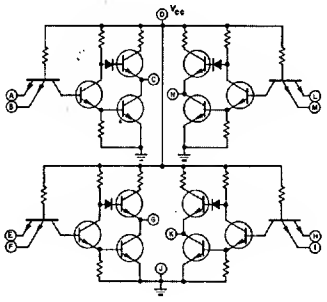
Quad 2-Input NAND/NOR Gate



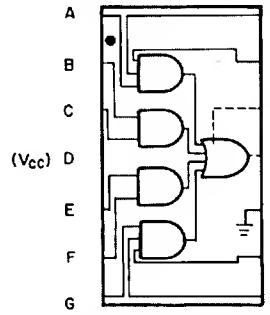
SG-140
SG-141
SG-142
SG-143

$C = \overline{(A \cdot B)}$ $K = \overline{(H \cdot I)}$

$G = \overline{(E \cdot F)}$ $N = \overline{(L \cdot M)}$

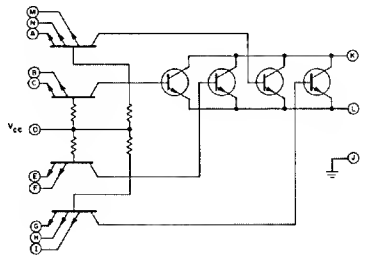


Quad 2-Input OR Expander

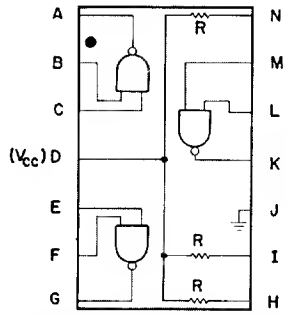


SG-150
SG-151
SG-152
SG-153

NOTE: USE IN CONJUNCTION WITH EXPANDABLE OR GATES.



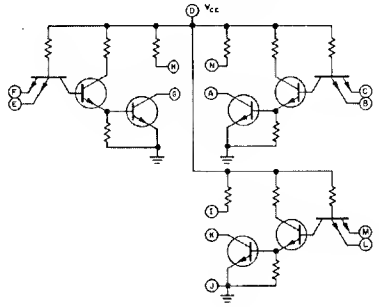
Triple 2-Input Bus Driver



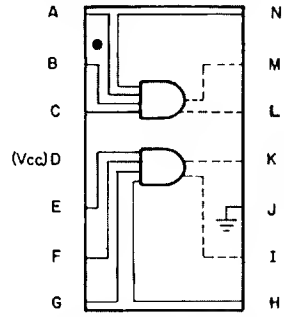
SG-160
SG-161
SG-162
SG-163

INDIVIDUAL: $A=\overline{(B\cdot C)}$; $G=\overline{(E\cdot F)}$; $K=\overline{(M\cdot L)}$

BUSSED : OUTPUT = "I" $=\overline{(B\cdot C)+(E\cdot F)+(M\cdot L)}$

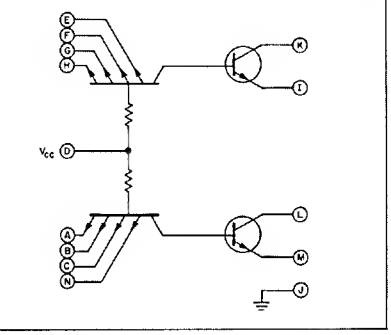


Dual 4-Input OR Expander

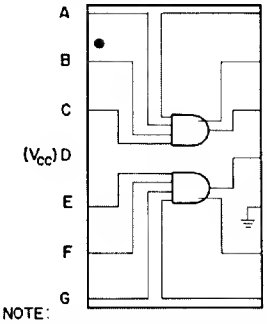


SG-170
SG-171
SG-172
SG-173

NOTE: USE IN CONJUNCTION WITH EXPANDABLE OR GATES.

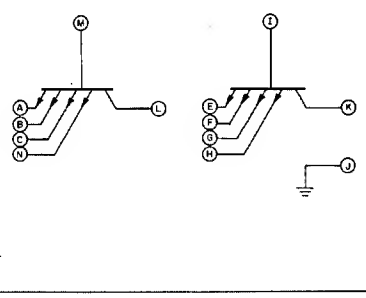


Dual 4-Input AND Expander

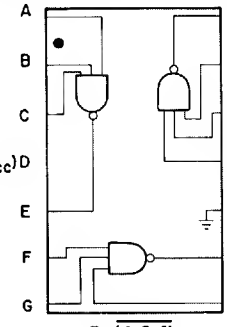


SG-180
SG-181
SG-182
SG-183

NOTE:
USE IN CONJUNCTION WITH EXPANDABLE SINGLE 8-INPUT NAND/NOR GATE.

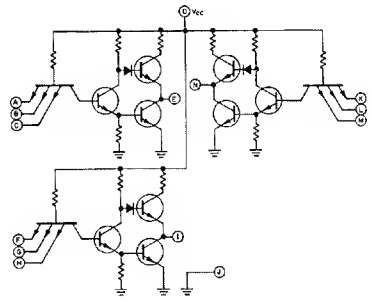


Triple 3-Input NAND/NOR Gate

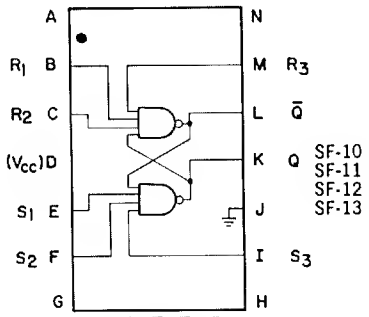


SG-190
SG-191
SG-192
SG-193

$E=\overline{(A\cdot B\cdot C)}$
$I=\overline{(F\cdot G\cdot H)}$
$N=(K\cdot L\cdot M)$

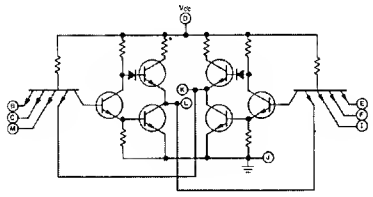


Set-Reset Flip-Flop

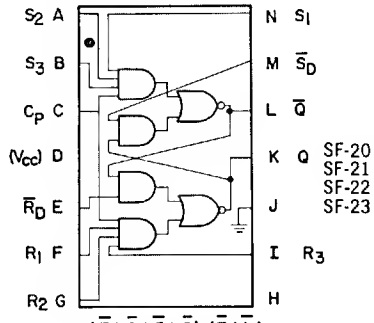


$L=(\overline{B}+\overline{C}+\overline{M}+\overline{K})$

$K=(\overline{E}+\overline{F}+\overline{I}+\overline{L})$

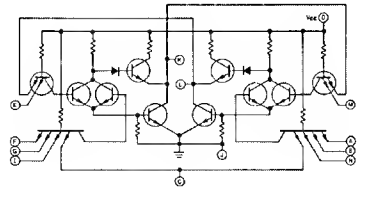


Two-Phase SR Clocked Flip-Flop

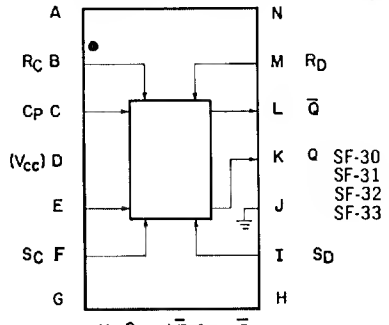


$K=(\overline{F}+\overline{G}+\overline{I}+\overline{C})\cdot(\overline{E}+\overline{L})$

$L=(\overline{A}+\overline{B}+\overline{N}+\overline{C})\cdot(\overline{M}+\overline{K})$

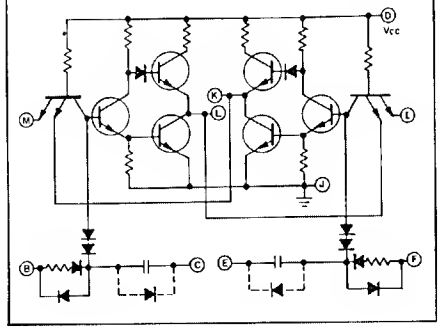


Single-Phase SRT Flip-Flop

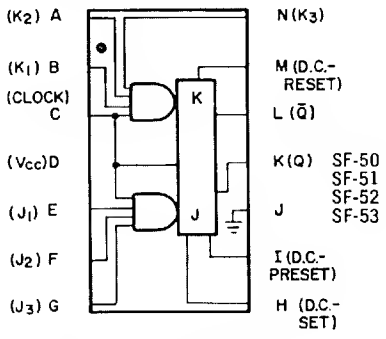


$K=Q_{n+1}=\overline{F}\cdot C_p+\overline{I}$

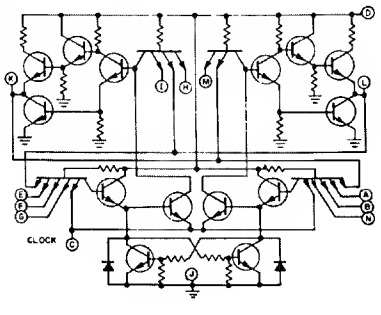
$L=\overline{Q}_{n+1}=\overline{B}\cdot C_p+\overline{M}$



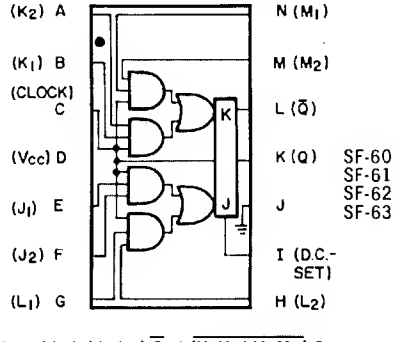
J-K Flip-Flop (AND Inputs)



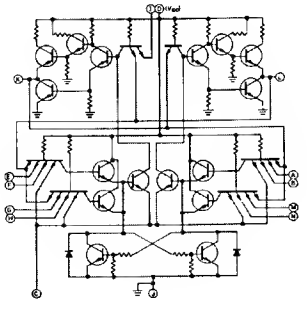
$Q_{n+1}=J_1\cdot J_2\cdot J_3\cdot\overline{Q}_n+\overline{K_1\cdot K_2\cdot K_3}\cdot Q_n$



J-K Flip-Flop (OR Inputs)



$Q_{n+1}=(J_1\cdot J_2+L_1\cdot L_2)\cdot\overline{Q}_n+\overline{(K_1\cdot K_2+M_1\cdot M_2)}\cdot Q_n$



This is SUHL-II . . . *Industry's Fastest Saturated TTL*

Sylvania's new line of high speed saturated digital logic circuits—SUHL-II—solves high speed system requirements without compromising system performance characteristics. Consisting of totally compatible 6 nanosecond gates and 30 megacycle J-K flip-flops, the new line is designed to operate from a single 5-volt power supply. All SUHL-II circuits have high noise immunity, fan-out, and capacitance drive capability. And, extra packages are not required to restore logic levels or noise margin at the system level.

Stable logic swings have been maintained through use of saturated logic. This results in stable propagation times over broad operating temperature excursions without recourse to additional bias supplies, complex loading rules, and external clamping and shielding. Also, low power OR expansion is accomplished without degradation of fan-out and without capacitively loading the gate output.

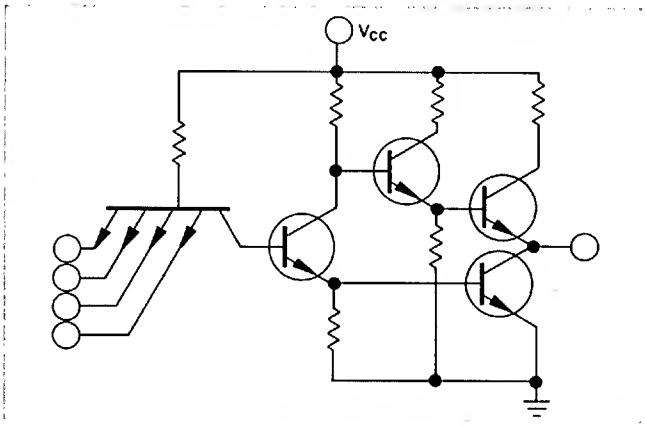
All SUHL-II circuits are totally compatible with and may be used in conjunction with all standard SUHL circuits.

The SUHL-II line is available in two package configurations: The Sylvania-designed 14-lead flat pack, and Sylvania's new hermetically sealed 14-lead plug-in package.

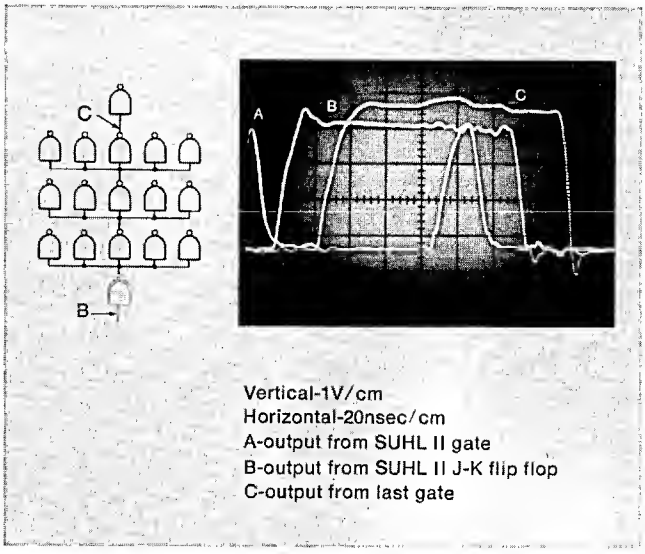
Features:

- High speed saturated logic:
  6 Nsec gates, 30Mc J-K flip-flops
- High noise immunity: $\begin{matrix}+1.0\\-1.5\end{matrix}$ Volt @ 25°V
- High logic swing: Logic "0"=0.25V
  Logic "1"=3.5V
- No logic level restorations necessary
- Single 5V power supply
- Two operating temperature ranges:
  Military −55°C to 125°C
  Industrial 0°C to +75°C
- Low power drain independent of fan-in or fan-out; typically 22MW/gate function
- Capacitance drive capability designed into *all* circuits
- No complex loading rules, inputs and outputs isolated
- Low output impedence, saturated logic; not subject to oscillations
- Low power wired-OR expansions without fan-out degradation
- Completely compatible with and can be intermixed with all standard SUHL circuits

SUHL-II Basic Circuit



SUHL-II speed



Vertical-1V/cm
Horizontal-20nsec/cm
A-output from SUHL II gate
B-output from SUHL II J-K flip flop
C-output from last gate

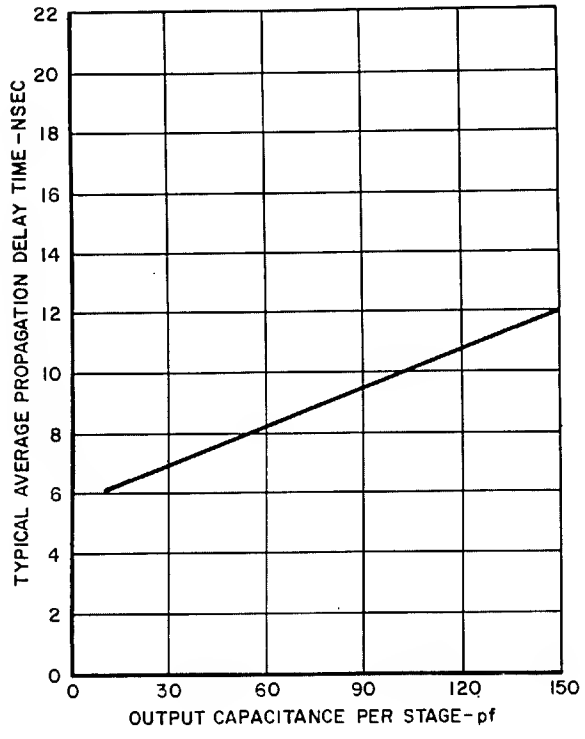
Typical Characteristics (+25°C, +5.0V)

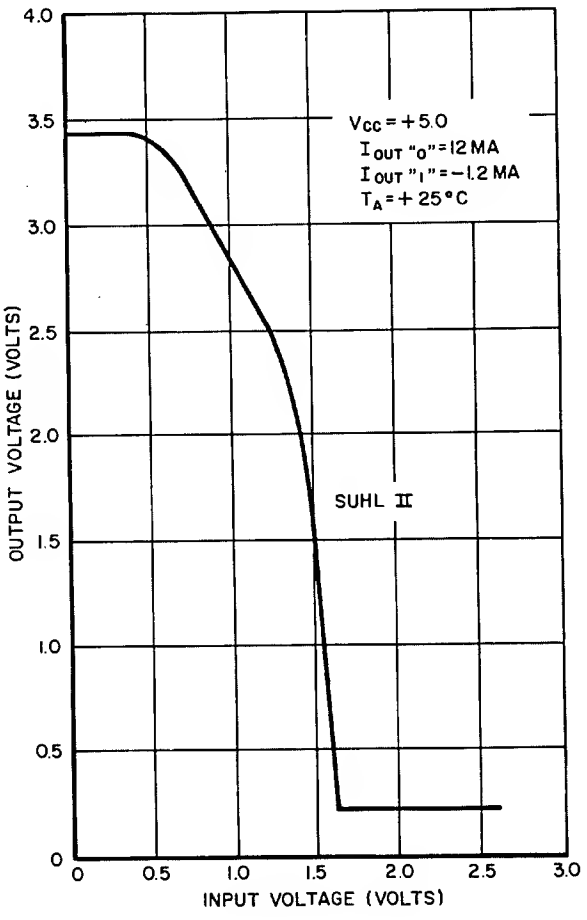
SUHL II TYPICAL CHARACTERISTICS (+25°C, +5.0 volts)

Function	Type Nos.	tpd (nsec)	Avg. Power (mw)	Noise Immunity +(volts)−		Military (−55° to +125°C) Prime FO	Military (−55° to +125°C) Std. FO	Industrial (0°C to +75°C) Prime FO	Industrial (0°C to +75°C) Std. FO
Expandable Dual 4-Input OR Gate	SG-210, SG-211, SG-212, SG-213	7	30	1.0	1.5	11	6	9	5
Quad 2-Input NAND/NOR Gate	SG-220, SG-221, SG-222, SG-223	6	22	1.0	1.5	11	6	9	5
Quad 2-Input OR Expander	SG-230, SG-231, SG-232, SG-233	2	28	1.0	1.5				
Dual 4-Input NAND/NOR Gate	S-240, SG-241, SG-242, SG-243	6	22	1.0	1.5	11	6	9	5
Expandable Quad 2-Input OR Gate	SG-250, SG-251, SG-252, SG-253	7.5	43	1.0	1.5	11	6	9	5
Single 8-Input NAND/NOR Gate	SG-260, SG-261, SG-262, SG-263	8	22	1.0	1.5	11	6	9	5
Dual 4-Input OR Expander	SG-270, SG-271, SG-272, SG-273	2	6.7	1.0	1.5				
J-K Flip-Flop (AND Inputs)	SF-250, SF-251, SF-252, SF-253	30mc	55	1.0	1.5	11	6	9	5
J-K Flip-Flop (OR Inputs)	SF-260, SF-261, SF-262, SF-263	30mc	55	1.0	1.5	11	6	9	5

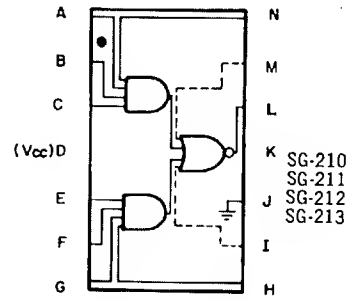
Typical Curves

AVERAGE PROPAGATION DELAY TIME
VS
CAPACITANCE LOADING
AT+5V, 25°C
SUHL II

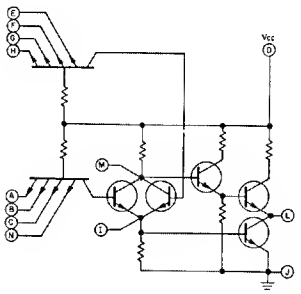




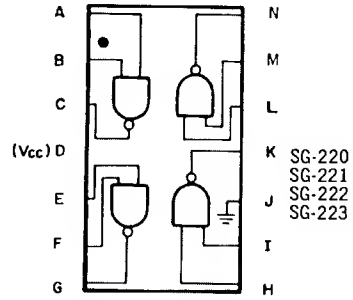
Expandable Dual 4-Input OR Gate



$L=\overline{(A\cdot B\cdot C\cdot N)+(E\cdot F\cdot G\cdot H)+--}$

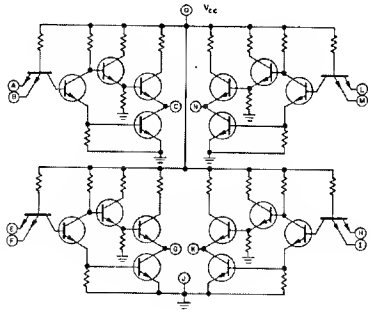


Quad 2-Input NAND/NOR Gate

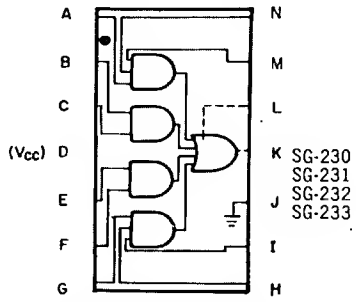


$C=\overline{A\cdot B}$ $K=\overline{H\cdot I}$

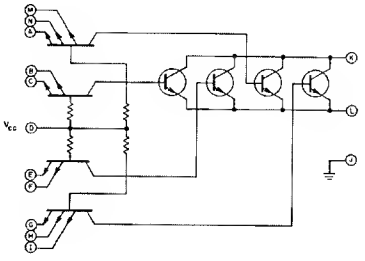
$G=\overline{E\cdot F}$ $N=\overline{L\cdot M}$



Quad 2-Input OR Expander



NOTE: USE IN CONJUNCTION WITH EXPANDABLE OR GATES.

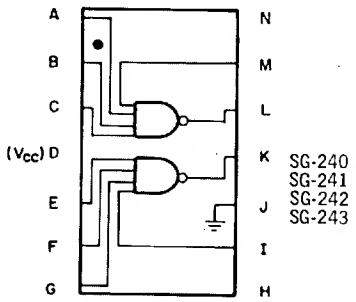


General Characteristics for all SUHL II Elements

ABSOLUTE MAXIMUM RATINGS				
	Military		Industrial	Unit
Supply Voltage	8		7	Vdc.
Operating Temperature	−55° to +125°		0° to +75°	°C
Storage Temperature	−65° to +200°		−65° to +200°	°C
Electrical Characteristics at 25° C, Vcc = 5V				
INPUT CHARACTERISTICS	**Min.**	**Typ.**	**Max.**	**Unit**
Logic 1 Voltage	1.7		5.5	Volts
Logic 1 Current			100	μA
Logic 0 Voltage			1.1	Volts
Logic 0 Current		1.7		mA
Capacitance		1.5		pf
Positive Noise Immunity[1]		1.0		Volts
Negative Noise Immunity		1.5		Volts
OUTPUT CHARACTERISTICS	**Min.**	**Typ.**	**Max.**	**Unit**
Logic 1 Voltage[2]	3.0	3.5	3.8	Volts
Logic 0 Voltage		0.26	0.45	Volts
Short Circuit Output Current[3]			65.0	mA
Propagation Delay Time/Gate (varies with element designed to be used up to 40 mc)		6	10	ns
Fan-Out	*varies with elements designed for fan-outs of 5 to 12*			

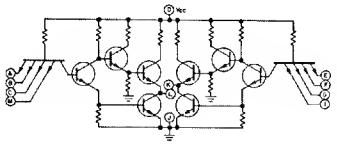
1. Noise immunity is that voltage superimposed on the input which will not propagate beyond the following stage. ■ 2. With max Vce (sat) on input. ■ 3. One second pulse.

Dual 4-Input NAND/NOR Gate

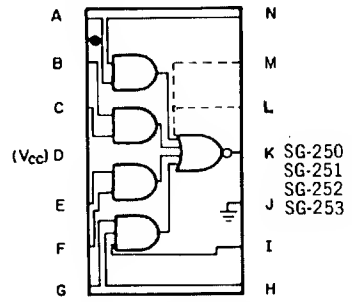


$L=\overline{A\cdot B\cdot C\cdot M}$

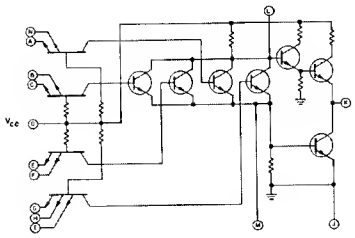
$K=\overline{E\cdot F\cdot G\cdot I}$



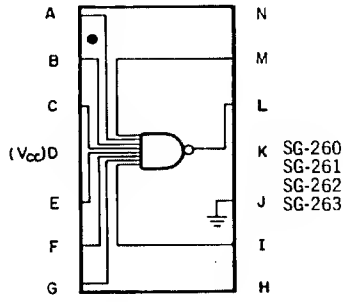
Expandable Quad 2-Input OR Gate



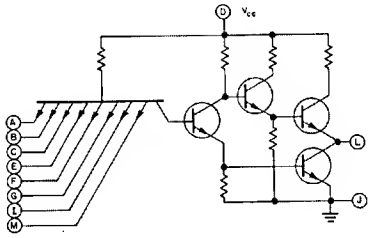
$K = \overline{A \cdot N + C \cdot B + E \cdot F + G \cdot H \cdot I}$



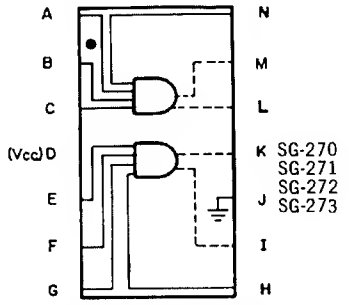
Single 8-Input NAND/NOR Gate



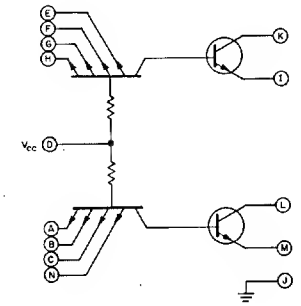
$L = \overline{(A \cdot B \cdot C \cdot E \cdot F \cdot G \cdot I \cdot M)}$



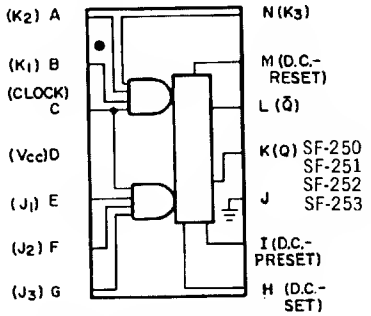
Dual 4-Input OR Expander



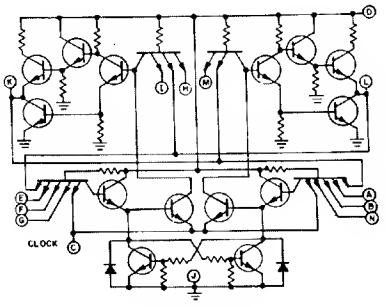
NOTE: USE IN CONJUNCTION WITH EXPANDABLE OR GATES.



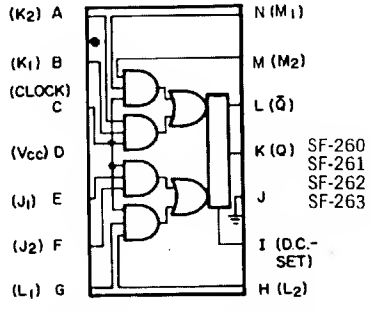
J-K Flip-Flop (AND Inputs)



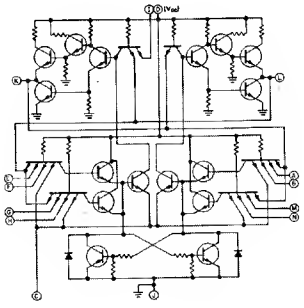
$Q_{n+1} = J_1 \cdot J_2 \cdot J_3 \cdot \overline{Q}_n + \overline{K_1 \cdot K_2 \cdot K_3} \cdot Q_n$



J-K Flip-Flop (OR Inputs)



$Q_{n+1} = \overline{(J_1 \cdot J_2 + L_1 \cdot L_2) \cdot \overline{Q}_n + (\overline{K_1 \cdot K_2 + M_1 \cdot M_2}) \cdot Q_n}$



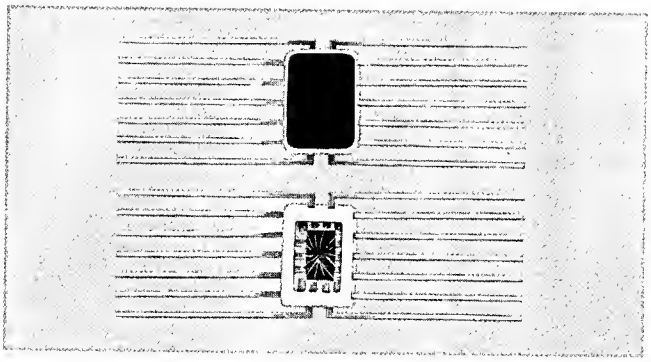
Packaging

All Sylvania Intergrated Circuits are available in two package configurations: the Sylvania-designed 14-lead flat pack and Sylvania's new Plug-in Package. Both alumina filled glass packages use high temperature glass seals. In addition, the package coefficient of expansion precisely matches that of the Kovar leads. All SUHL-I and SUHL-II integrated circuits are manufactured under super-clean and controlled ambient conditions to insure highest reliability. Assembly is accomplished with an all aluminum wire-bonding system that completely eliminates unpredictable "opens" caused by the formation of an inter-metallic compound, popularly referred to as "Purple Plague," which occurs when gold is bonded to aluminum in the presence of silicon.

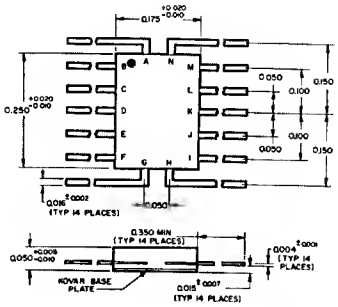
Every sealed circuit is sequentially processed through +300°C temperature aging, −55°C to +125°C temperature-cycling, 20,000 g centrifuge and leak testing to assure the user of the highest degree of product integrity.

14 Lead Flat Pack

Sylvania's new 14-lead flat pack is manufactured using high temperature, hard glass seals. The monolithic chips are brazed directly to a Kovar base plate providing a thermal resistance of 0.1°C/mw from junction to case. Pin connections are designed for optimum systems simplification with regard to inputs, outputs and cross-overs. Further, the same pin numbers are used for B+ and ground on every circuit, and these power-supply and ground pins are offset to avoid burn-out if the package is inadvertently mounted upside down.

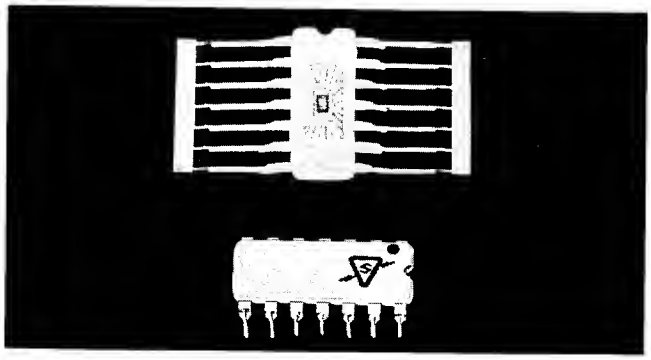


14 Lead Flat Pack

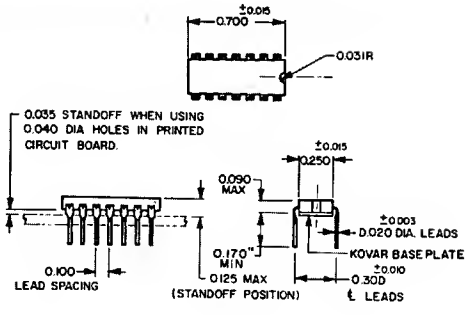


Sylvania Plug-in Package

Sylvania's new Plug-in Package is specifically designed for low cost assembly in two-sided printed circuit boards. The alumina filled glass package provides extremely low thermal resistance and features a Kovar base plate with up-from-the-chip bonding and gold plated Kovar leads formed into a 0.020″ diameter for both strength and reliable solderability. The 100 mil pin centers permit both broad drill tolerances and wide printed circuit lines while the leads provide a 0.035″ standoff for venting. The SUHL plug-in package leads form two seven pin rows, 300 mils apart along the sides of the package. Consequently, an installed package is readily accessible for in-place checkout.

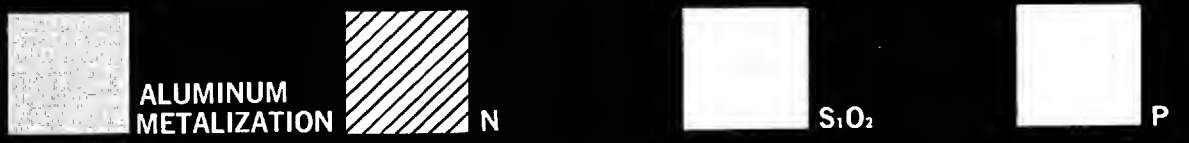


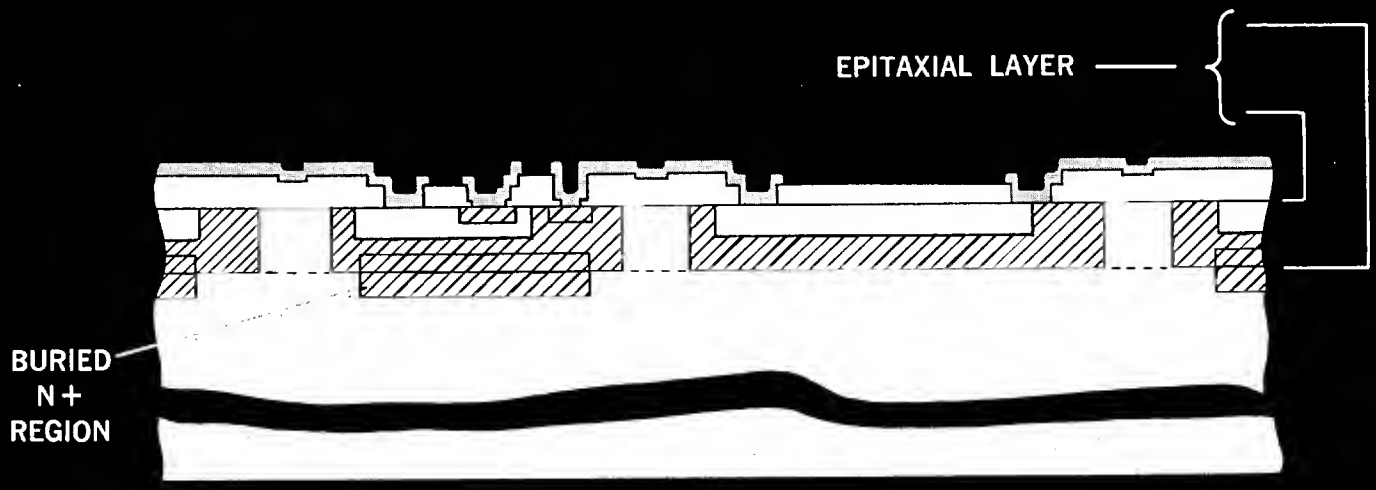
Sylvania Plug-in Package



Every sealed SUHL Circuit is 100% sequentially processed through the following Quality Control Tests:

- **Stabilization Bake . . . .** for 60 hours at 300°C to stabilize surfaces and to stress the package
- **Thermal Cycling . . . .** 5 cycles consisting of plunging the package into −55° and +125° air ambient. This test stresses the assembly on a cyclic basis.
- **Centrifuge . . . . . .** 20,000 g's in Y_1 plane to stress leads and seal
- **Oil Bubble Leak Test . . .** at 150°C to test hermeticity
- **DC Testing . . . . . .** to check all DC parameters at rated temperatures
- **AC Testing . . . . . .** to check switching parameters





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